10. Experimental Results with BP and PLL at FSK 23 kHz

UFO Doctor, Dec. 8th, 2011

1. Introduction

The Duck Project requires a Band Pass Filter for the Ultrasonic Signals 21.739 and 24.390 kHz (in order to attenuate the environmental noise)
The filtered signals are processed by a PLL (Phase Lock Loop) with a lock-in range in the order of 21 to 25 kHz.
This report shows the V4 experimental result on a Wire Wrap bread board circuit:

2. Circuit V4 for Dual HP, single BP and PLL

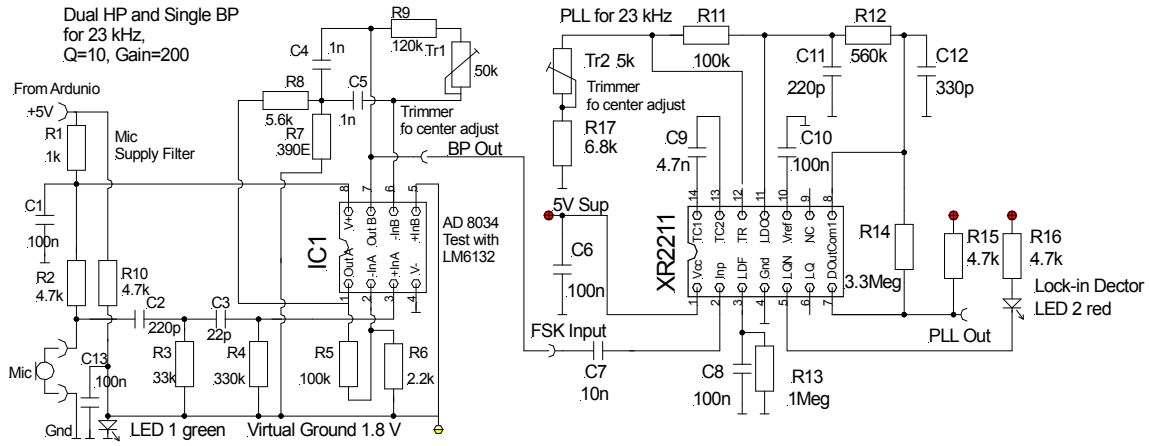

Fig. 1: Circuit BP and PLL

3. Frequency Response of the Band Pass Filter

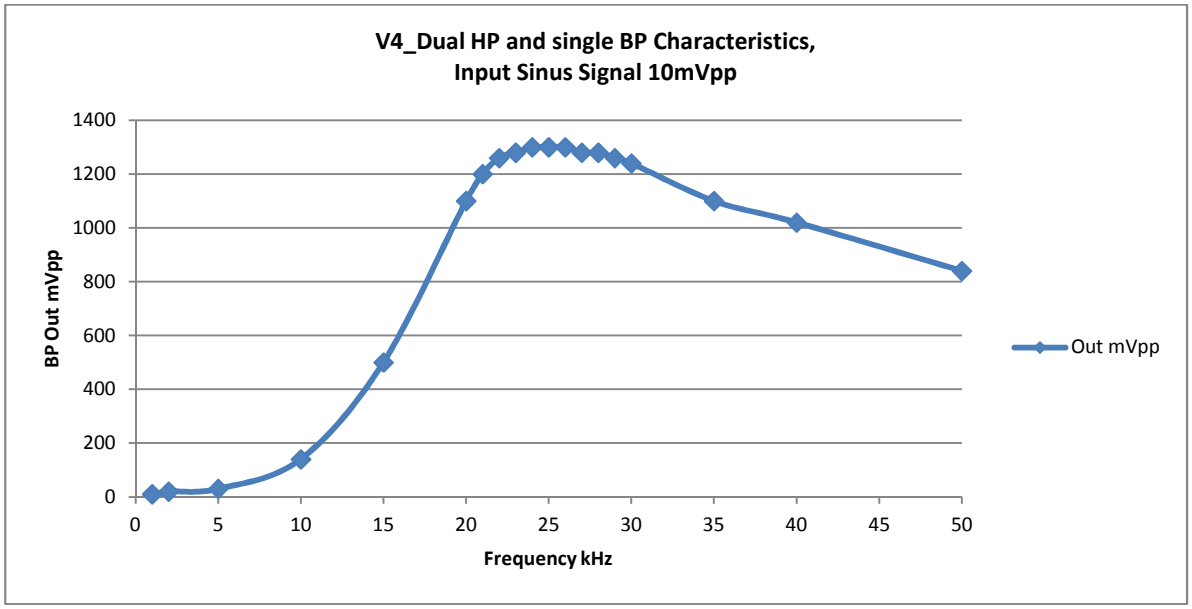

Fig. 2. Frequency Response of the Band Pass.
We see here a gain of about 130, (simulation: 220), but this is ok since this experiment was done with a low power DIL Opamp LM6132 instead of the actual SMD IC AD8034

4. FSK Discrimination

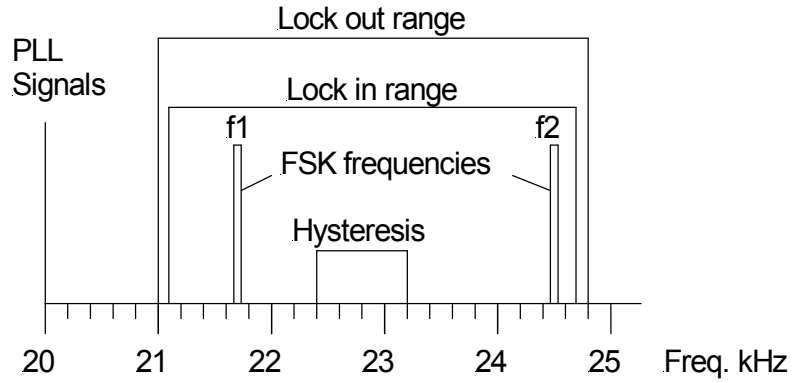

Fig. 3. FSK discrimination and Lock-in Range of the PLL

5. Discussion:

The BP and PLL performance is ok.

6. HP_BP Computation with EXCEL

	A	B	C	D	E
1	V4 High Pass and Band Pass Calculation				
2	PAN, 07.12.2011				
3	Literature: Tietze Schenk, 1980, page 14 and 308				
4					
5	Number Pi	3.14156			
6	fo	23065	Hz		
7					
8	Highpass for fo, Noninv. Amp				
9	Parameter	Calc. Value	Selected Value	Units	Formula
10	Cut off Fc	23065		Hz	Choose a frequency
11	C	2.20E-10	220pF	F	First free Selection
12	Imp C at fc	3.14E+04	31k	jOhm	Z=1/(2*Pi* fc*C)
13	R	3.14E+04	33k		R=1/(2*Pi*C*fc)
14					
15	2nd Test Highpass for fo, Noninv. Amp				
16	Parameter	Calc. Value	Selected Value	Units	Formula
17	Cut off Fc	23065		Hz	Choose a frequency
18	C	2.20E-11	22 pF	F	First free Selection
19	Imp C at fc	3.14E+05	310k	jOhm	Z=1/(2*Pi* fc*C)
20	R	3.14E+05	330k		R=1/(2*Pi*C*fc)
21	Gain A1	44.00	(22 at fo!)		Select a value for gain
22	R4	1.00E+05	100k		Select a value for RN
23	R5	2.33E+03	2.2k		R5= RN/(A-1)
24					
25	Band Pass for fo				
26	Parameter	Comp Value	Selected Value	Units	Formula
27	Center fc	23065		Hz	Choose a frequency
28	R1	5610.04152	5.6k	Ohm	R1=R2/(-2*A)
29	R2	1.38E+05	120kfix+50kTrim	Ohm	R2=Q/(Pi*Fc*C)
30	R3	367.626589	330+33	Ohm	R3=-A*R1/(2*Q^2+A)
31	C	1.00E-09	1n	F	First free Selection
32	Q	10			Second Selection
33	Gain A2	-12.3			Third Selection

Fig. 4: Computation HP_BP

7. PLL Computation and Experiment

	A	B	C	D	E
1	V4 PLL Calculations for FSK frequencies in the 20-30kHz range				
2	UFO Doctor, Dec 7th, 2011				
3	Related Documents: EXAR Doc XR-2211, June 1997-3				
4	Circuit: Fig. 3 on Page 7				
5	Design Equations, page 10				
6	X'= calculated value, X selected value				
7	Comment 1: The minimum Ro is 10kOhm for good temperature stability				
8	Element	Value	Unit	Formula	Comment
9	Baud Rate	1200	1/s		above 1000
10	f1	21739	Hz		your wish
11	f2	24390	Hz		your wish
12	fo	23026	Hz	fo= SQRT (f1*f2)	central frequency
13	Delta FSK	2651	Hz	Delta FSK=f2-f1	+/- 5.7%
14	Ro'	10000	Ohm		Recommended
15	Co'	4.34E-09	F	Co'=1/(Ro*fo)	First choice
16	Co	4.70E-09	F	4.7nF	Selected
17	Ro	9.24E+03	Ohm	Ro=1/(Co*fo)	at center frequency
18	Ro fix	6800	Ohm	6.8k	Selected
19	Ro trim	5000	Ohm	Rtrim= about Ro/2	Selected
20	Ro mean	9300	Ohm	Ro mean=R0 fix+0.5Ro trim	at trim center
21	R1'	160518	Ohm	R1'=2*(Ro*fo)/(f2-f1)	tracking bandwitdh
22	R1''	107012	Ohm	R1'/1.5	reduction by 1.5
23	R1	100000	Ohm	100k	Selected
24	Eta	0.5			Recommended
25	C1'	2.35E-10	F	C1'=(1250*Co)/R1*Eta^2)	Loop damping
26	C1	2.20E-10	F	220pF	Selected
27	RF'	500000	Ohm	RF'=5*R1	min 5*R1
28	RF	560000	Ohm	560k	Selected
29	RB'	2800000	Ohm	RF'=5*RF	min 5*RF
30	RB	3300000	Ohm	3.3Meg	selected
31	Rsum'	550000	Ohm	Rsum'=(RF+R1)*RB/(RF+R1+RB)	Calc Rsum
32	Rsum	688489	Ohm		Selected
33	CF'	3.03E-10	F	CF'=0.25/(Rsum*Baud Rate)	Calc CF
34	CF	3.30E-10	F	330pF	Selected
35	Carrier Detect				
36	Tau	1.00E-01	s	0.1sec	your wish
37	CD	1.00E-07	F	100nF	your selection
38	RD'	1.00E+06	Ohm	RD'=Tau/CD	Calc RD'
39	RD	1.00E+06	Ohm	1Meg	Selected
40					
41	Experimental results				Status
42	lower lock out	21	kHz		ok
43	lower lock in	21.1	kHz		ok
44	f1 detect	22.4	kHz		ok
45	f2 detect	23.2	kHz		ok
46	upper lock in	24.7	kHz		ok
47	upper lock out	24.8	kHz		ok
48	Sig Hysteresis	0.8	kHz	Hyst= f2det-f1det	ok
49	Tracking BW	3.6	kHz	upper to lower lock in	ok

Fig. 5: Computation and Experiments on PLL