93. IR PWM Generator 15.6kHz, 9 W and US FSK Burst Generator 38/41kHz, 0.2W **Draft 1.1**

UFO Doctor, May 25th, 2015

1. Introduction

The investigation of directivity characteristics of IR-Diodes and US-Mics requires:

- an IR PWM Generator for 6x1.5 Watt IR-LED, 15.6kHz, PWM 1 to 50% Duty Cycle,
- an US FSK Generator for 0.2W US Speaker, FSK 39/41kHz.

We show here the concepts, the simulations and the first experimental results

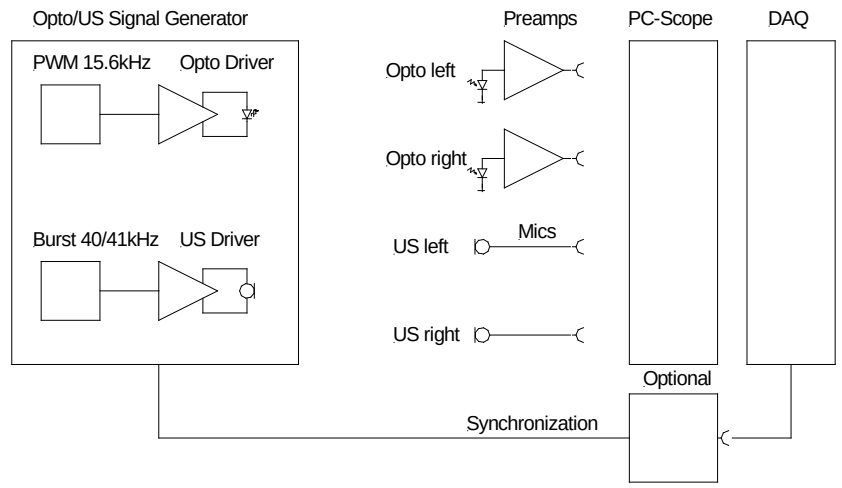

Fig. 1: Test Setup

The Opto/US Signal Generator is a standalone unit with a 2-Cell Lipo.

The received signals will be displayed and analyzed by a PC Scope.

The Signal Generator might be synchronized by wire or RC with the DAQ

2. PWM Generator

2.1. Concept

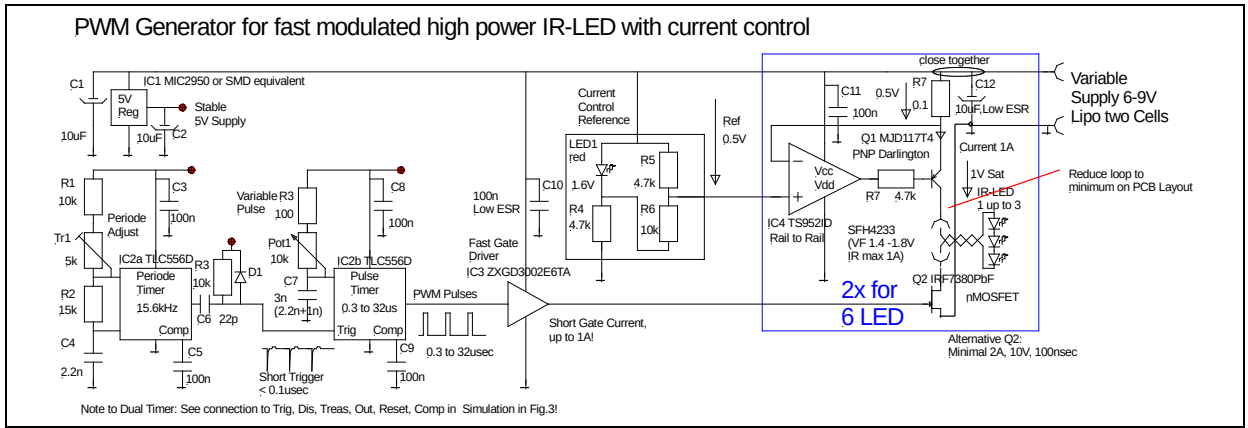

Fig. 2: 15.6 kHz Generator with 1 to 50 % Duty Cycle, important: C12 low ESR near R7

Comments:

The trigger for the Pulse Timer must be shorter than its minimum pulse duration.

The short 2x1A pulses will cause EMC problems. We propose following counter measures:

- Short cable to Lipo, Block Capacity, low ESR, very close to shunt R7
- Twisted cable to the 2x3 IR-LED

2.2. Opto Timer Simulation

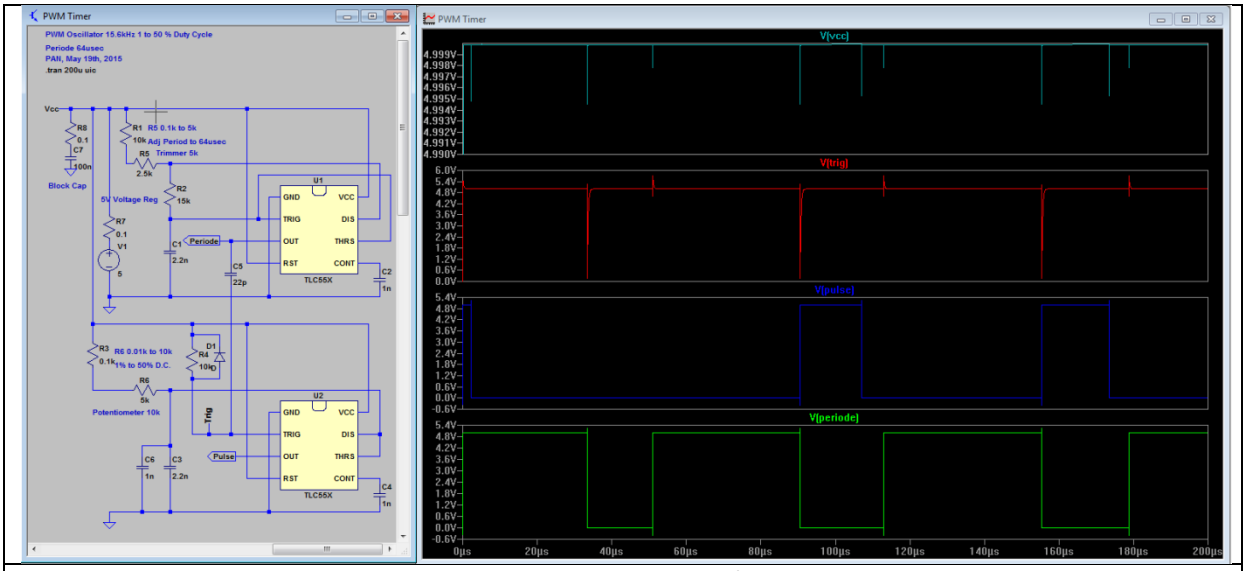

Fig. 2: Timer simulation with TLC-555 Timers, Period 64usec/15.6kHz, Pulse here 50% D.C
Top: Supply Distortion at Vcc, Blocked by 100nF, less than 10mV, ok.
Middle: Trigger Pulse, should be shorter than 0.1us, ok.
Middle: Pulse, Set to 50% D.C., ok.
Below: Period, set to 64us, ok.

Comment: The first timer period is never correct with any 555 Timer!
This has to do with charging of the timer capacitors C1 to the lower 1/3 Vcc threshold during DC supply start!

2.3. Opto IR PWM Simulation

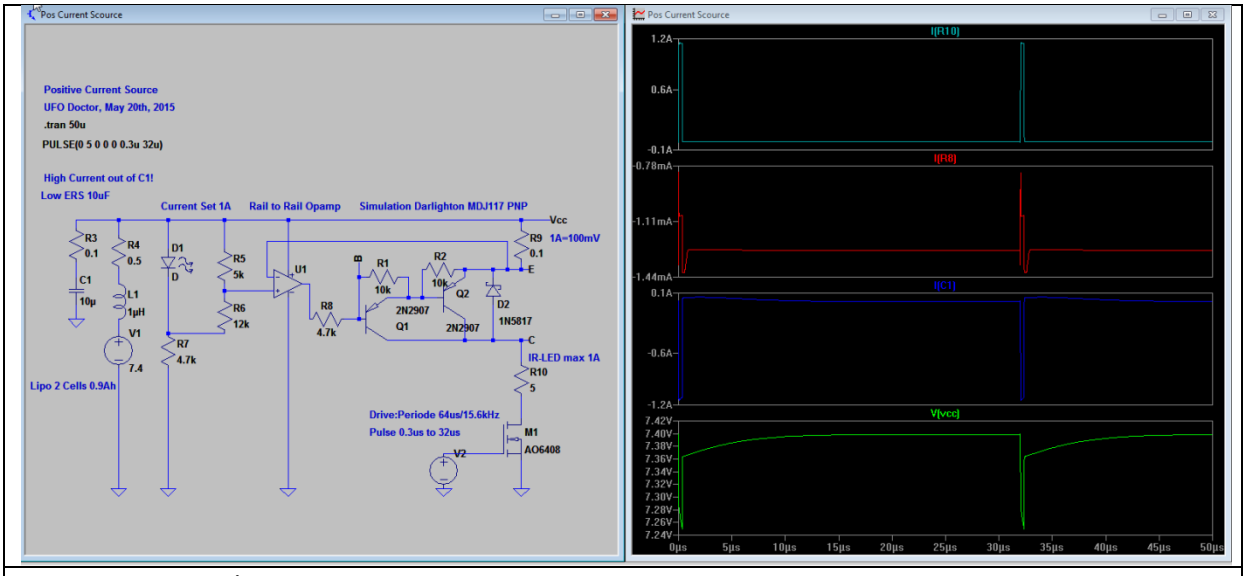

Fig. 3: Driver Simulation
Top: Current into 3 serial 1A-IR-LED, simulated by a 5 Ohm resistor, ok
Middle: Current from Opamp U1 to drive the simulated PNP Darlington, <2mA, ok
Middle: Current from block Capacitor C1: 1A!; find a 10uF capacitor with VERY LOW ESR!
Below: Vcc Supply Distortion caused by short 1A pulses, less 0.3V with a good block capacitor C1, ok

3. US-FSK Burst Generator

3.1. Circuit

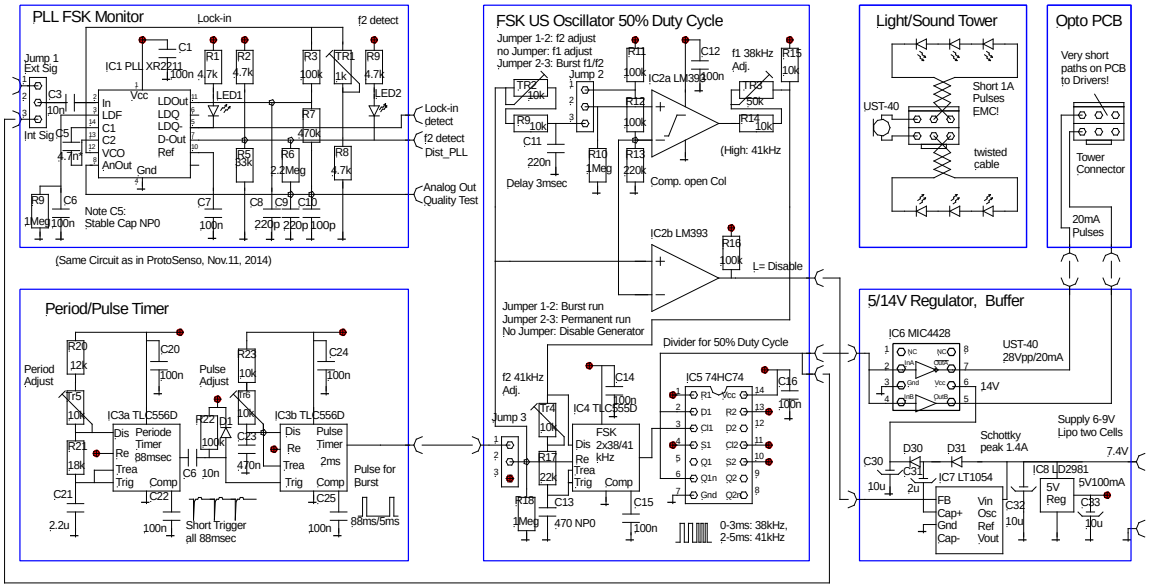

Fig. 4: Circuit US- FSK Burst Generator

3.2.Timer Simulations

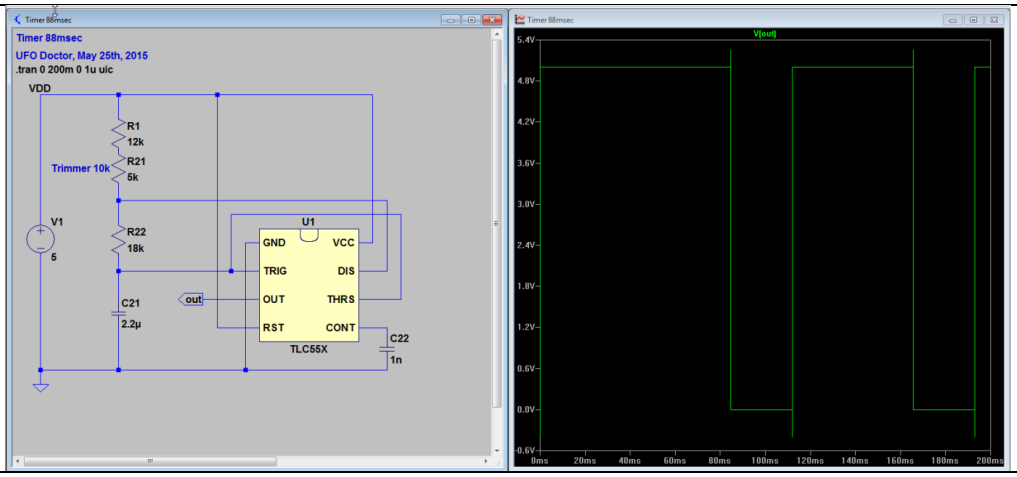

Fig. 5:Timer 88msec

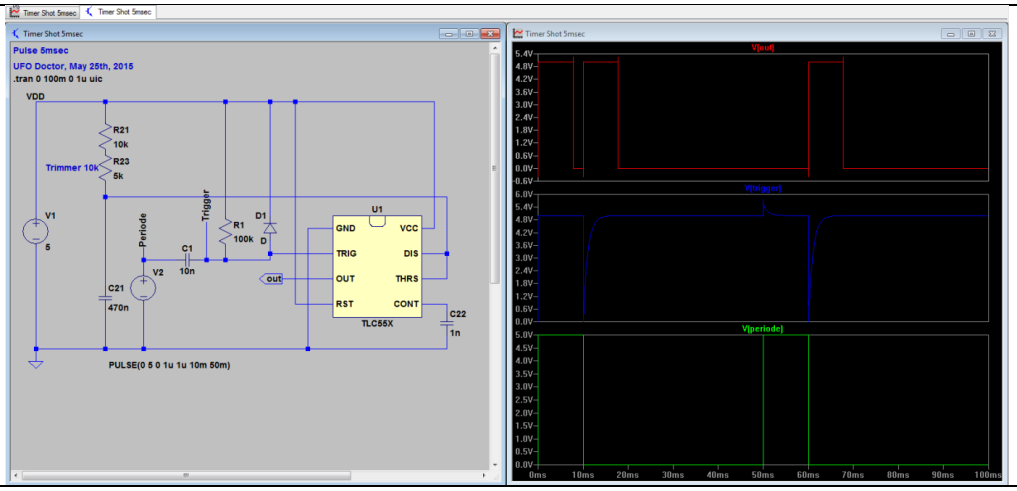

Fig. 6: Single Shot 5msec for burst period

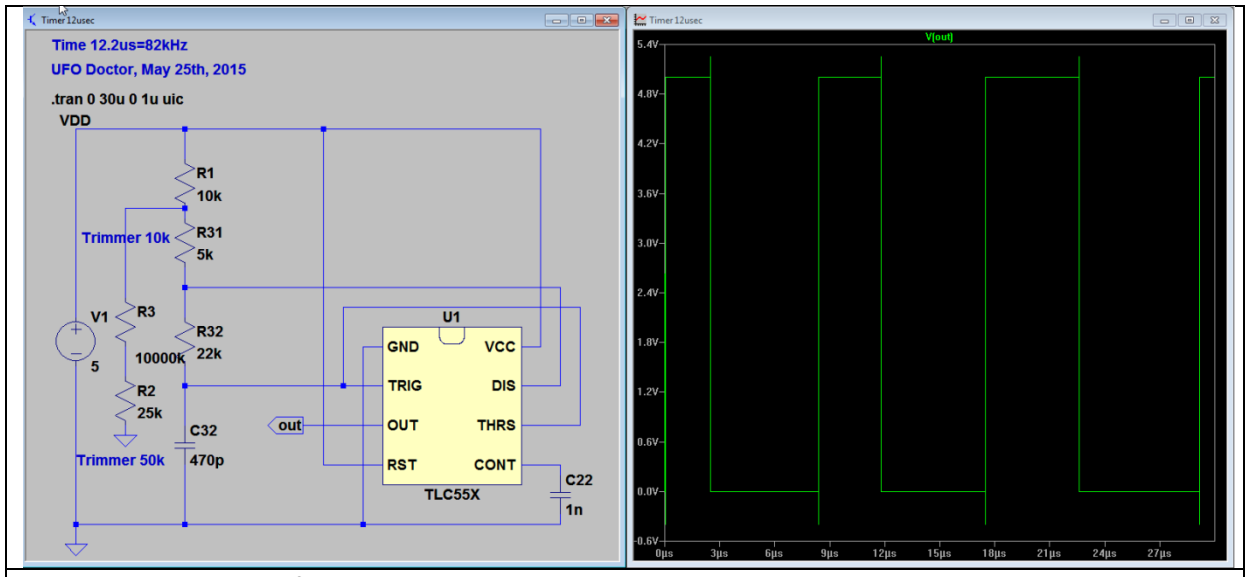

Fig. 7: Timer 12.2 usec for 2x 41kHz, Bypass R3, R2 disabled

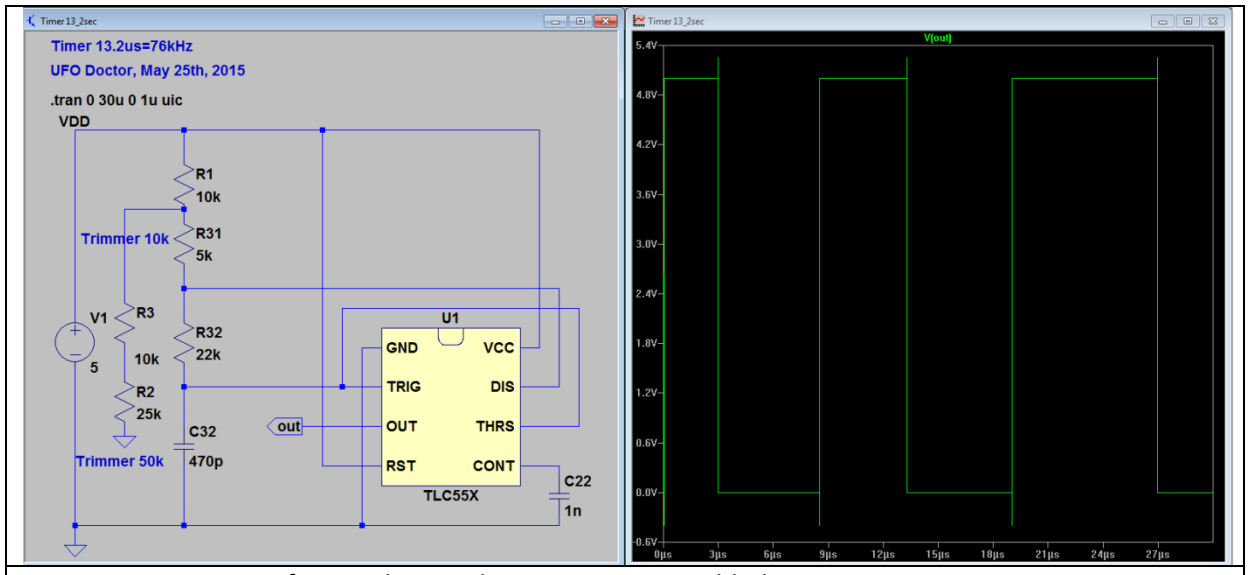

Fig. 8: Timer 13.2usec for 2x38kHz, with Bypass R3, R2 enabled

3.3. Simulation FSK Burst

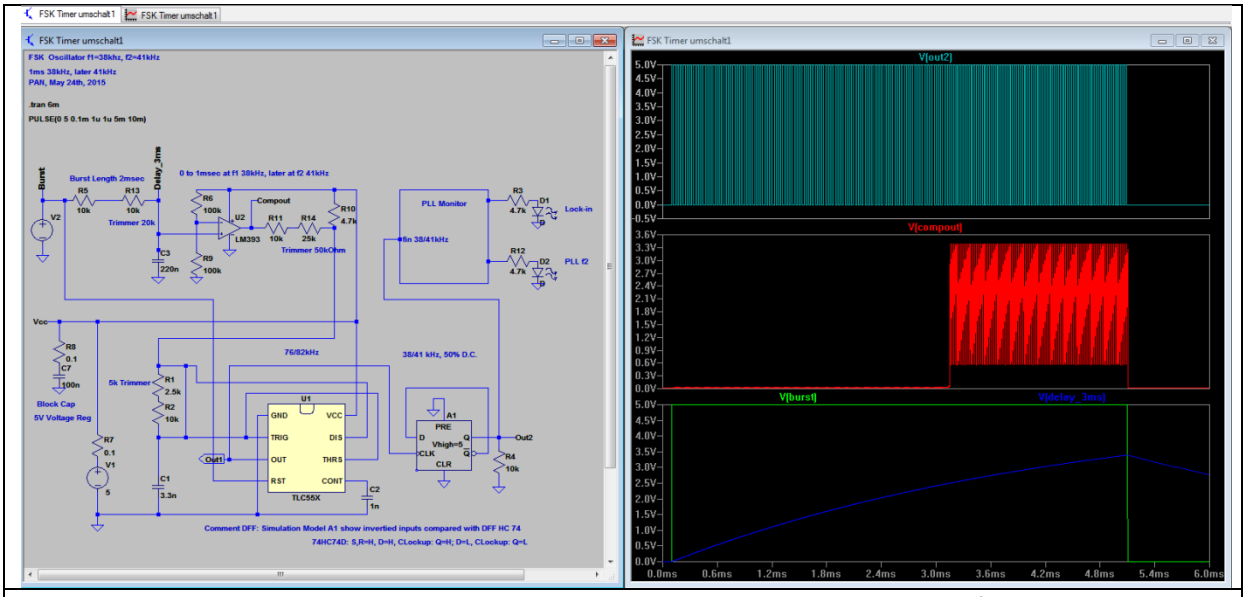

Fig. 10: Burst 5 msec all 88msec, FSK beginning with 38kHz, switching to 41kHz after 3ms
Top: FSK Output, 38/41kHz, 50% Duty Cycle by D-FF
Middle: Comparator Output
Below: Burst Input and Delay Ramp

3.4. Simulation Voltage Doubler with Shut Down and Buffer for UST-40 Speaker

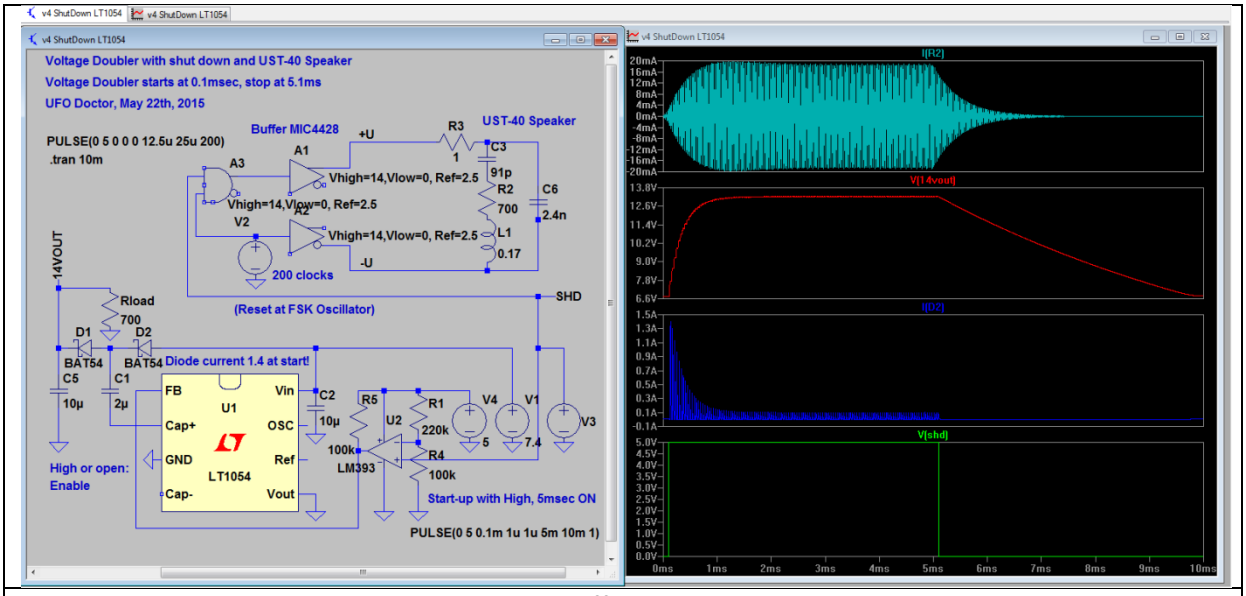

Fig. 11: Voltage Doubler with Shut Down and Buffer at UST-40 Speaker
Top: Current through speaker, +/-20mA, ok
Middle: Output Voltage Doubler
Middle: Current through Diodes D1, D2 1.4A at start, select appropriate Schottky diodes!
Bottom: Pulse Burst Duration, about 5msec